REMARKS/ARGUMENTS

Claims 1-15 are pending in the present application. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 103, Obviousness

The Examiner has rejected claims 1, 2, 5, 6, 8, 9, 12, 13, 14 and 15 under 35 U.S.C. § 103(a) as being unpatentable over *Callway*, Dynamic Component to Input Signal Mapping System, U.S. Patent No. 6,950,772 B1, September 27, 2005 (hereinafter *Callway*), in view of *Conner*, Tester for LSI Devices and Memory Devices, U.S. Patent No. 4,450,560, May 22, 1984 (hereinafter *Conner*). This rejection is respectfully traversed.

Applicants' claims 1 and 8 describe a plurality of multiplexers receiving specific test signals. These multiplexers combine test signals received for each test signal group to create a plurality of test signal groups. Mapping logic then receives one of the test signal groups from each one of the multiplexers. The mapping logic then maps one of the test signal groups to any one of the outputs of the mapping logic to output as a test output group.

The Examiner states that *Callway* teaches all of the features of these claims except for test signal groups. The Examiner relies on *Conner* to teach test signal groups.

The Examiner does not point to any particular element within *Callway* that is supposedly analogous to Applicants' claimed mapping logic. It appears that the Examiner may be asserting that the entire dynamic component of *Callway* is analogous to Applicants' mapping logic. Figure 2 of *Callway* depicts the entire dynamic component. The entire dynamic component, however, is not analogous to the mapping logic claimed by Applicants.

The dynamic component outputs signals from output multiplexer 228. For *Callway* to teach Applicants' claimed mapping logic, the dynamic component of Figure 2 of *Callway* must map signals to any one of the outputs of the output multiplexer 228. *Callway* does not teach mapping signals to any one of the outputs of the output multiplexer 228. *Callway* teaches the signal analyzer 238 mapping connections of the components 208, 210, 212 to the output ports. *Callway* does not, however, teach that the connections can be mapped to any one of the output ports of output multiplexer 228.

Callway does not teach or suggest mapping, by mapping logic, one of the connections of the components 208, 210, 212 to any one of the output ports of output multiplexer 228. *Callway* teaches the dynamic component being used in a chip that inputs YPrPb and composite video signals. One example of an environment where such a chip can be used is to input television signals. *Callway* teaches that the components 208, 210, 212 are A/D converters. A composite video signal needs an A/D converter that has

excellent linearity. The dynamic component of *Callway* can be used to select the A/D converter that has the best linearity for processing the composite video signal. The other two A/D converters are then used to process the YPrPb signals.

Callway suggests that the outputs of the dynamic component are then provided to the rest of the device which includes the dynamic component. The rest of the device will be expecting the composite video signal to be output from the dynamic component always using the same output port. The rest of the device will not be expecting the dynamic component to change which output port it uses to output the composite video signal. Indeed, *Callway* does not teach that signals, such as composite signals, are output using any one of the outputs. *Callway* appears to suggest that signals, such as composite signals, are output using the same output port.

Using composite video signals as an example, suppose A/D converter 210 is selected for the composite video signal because it has the best linearity. If the device that includes the dynamic component is expecting a composite video signal to be output from output port 204, the composite video signal is received by output mux 228 from A/D converter 210 and then output using output port 204. If, on the other hand, A/D converter 208 is selected because it has the best linearity, the composite video signal is received by output mux 228 from A/D converter 208. Because it is reasonable to assume that the rest of the device is still expecting the composite video signal to be output from output port 204, output mux 228 will receive the composite video signal from A/D converter 208 and output that signal through output port 204. Thus, *Callway* suggests that the signal received by output mux 228 is not output to any one of its output ports. It is output to the same output port.

Callway does not teach mapping signals to any one of the outputs of the output multiplexer 228. *Callway* teaches the signal analyzer 238 mapping connections of the components 208, 210, 212 to the output ports, but is silent as to how output ports are selected for outputting signals that are received by the output multiplexer. Therefore, *Callway* does not suggest mapping, by mapping logic, one of the connections to any one of the output ports.

Because *Callway* does not teach or suggest the entire dynamic component receiving, by mapping logic, one of said plurality of test signal groups from each one of said plurality of multiplexers; and mapping, by said mapping logic, one of said plurality of test signal groups to any one of a plurality of outputs of said mapping logic to output as a test output group, *Callway* does not teach or suggest the features of Applicants' claims as asserted by the Examiner.

If the Examiner is asserting that the output multiplexer 228 is analogous to Applicants' mapping logic, *Callway* does not teach the features of Applicants' claims. The output multiplexer 228 is not analogous to Applicants' mapping logic for the reasons given above. *Callway* does not teach mapping signals to any one of the outputs of the output multiplexer 228. *Callway* teaches the signal analyzer 238

mapping connections of the components 208, 210, 212 to the output ports of output multiplexer 228. *Callway* does not, however, teach that the connections can be mapped to any one of the output ports.

If the Examiner is asserting that the mapping module 251 of *Callway* is analogous to Applicants' mapping logic, *Callway* does not teach the features of Applicants' claims. Mapping module 251 receives a single input. That input is input into signal analyzer 238. The mapping module 251 of *Callway* does not receive multiple input signals. Applicants claim receiving, by mapping logic, one of said plurality of test signal groups from each one of said plurality of multiplexers. Because *Callway* does not teach the mapping module 251 receiving multiple signals, *Callway* does not teach mapping logic receiving a test signal group from each multiplexer. Therefore, *Callway* does not teach the features of Applicants' claims.

Applicants also claim receiving test signals by a plurality of multiplexers. These test signals are combined by the plurality of multiplexers to create a plurality of test signal groups. The mapping logic then receives one of the test signal groups from each one of the plurality of multiplexers. The mapping logic then maps one of the test signal groups, received from one of the plurality of multiplexers, to any one of the outputs of the mapping logic. The Examiner relies on *Callway* to teach these features.

If the Examiner is asserting that the entire dynamic component of *Callway* is the mapping logic claimed by Applicants, *Callway* does not teach receiving specific test signals by a plurality of multiplexers. *Callway* does teach a single input multiplexer, but does not teach a plurality of input multiplexers. Therefore, if the entire dynamic component of *Callway* is believed to be the mapping logic claimed by Applicants, *Callway* does not teach receiving specific test signals by a plurality of multiplexers.

Callway also does not teach combining, by a plurality of multiplexers, the test signals received for each test signal group; and does not teach receiving, by mapping logic, one of said plurality of test signal groups from each one of said plurality of multiplexers because *Callway* does not teach a plurality of input multiplexers.

If the Examiner is asserting that the output multiplexer 228 of *Callway* is the mapping logic claimed by Applicants, *Callway* does not teach receiving specific test signals by a plurality of multiplexers. *Callway* does teach a single input multiplexer, but does not teach a plurality of input multiplexers. Therefore, if the output multiplexer 228 of *Callway* is believed to be the mapping logic claimed by Applicants, *Callway* does not teach receiving specific test signals by a plurality of multiplexers.

If the Examiner is asserting that the mapping module 251 of *Callway* is the mapping logic claimed by Applicants, *Callway* does not teach receiving specific test signals by a plurality of multiplexers. *Callway* does teach a single input multiplexer, but does not teach a plurality of input

multiplexers. Therefore, if the mapping module 251 of *Callway* is believed to be the mapping logic claimed by Applicants, *Callway* does not teach receiving specific test signals by a plurality of multiplexers.

The Examiner relies on *Conner* to teach test signal groups. *Conner* teaches a group of test signals, but does not cure the deficiencies of *Callway* that are discussed above. Therefore, the combination of *Callway* and *Conner* does not render Applicants' claims obvious.

Neither *Callway* nor *Conner* describes, teaches, or suggests a plurality of multiplexers that combine test signals to create a plurality of test signal groups. Neither *Callway* nor *Conner* describes, teaches, or suggests mapping logic that receives one of the test signal groups from each one of the multiplexers or mapping logic that maps one of the test signal groups to any one of the outputs of the mapping logic to output as a test output group.

Because neither *Callway* nor *Conner* describes, teaches, or suggests, either singly or in combination, the features of claims 1 and 8, the combination of *Callway* and *Conner* does not render claims 1 or 8 obvious.

Claims 5 and 12 describe the mapping logic including a plurality of mapping multiplexers. Each one of the mapping multiplexers receives the plurality of test signal groups. Each one of the mapping multiplexers generates a different one of the outputs of the mapping logic. Each one of the mapping multiplexers selects one of the test signal groups to output as a test output group.

Thus, according to Applicants' claims, there are two different multiplexers; there is a plurality of multiplexers, and the mapping logic includes a plurality of mapping multiplexers.

Neither *Callway* nor *Conner* describes, teaches, or suggests mapping logic that includes a plurality of mapping multiplexers. Neither reference describes, teaches, or suggests each one of the mapping multiplexers receiving the plurality of test signal groups and generating a different one of the outputs of the mapping logic where each one of the mapping multiplexers selects one of the test signal groups to output as a test output group.

Because neither *Callway* nor *Conner* describes, teaches, or suggests, either singly or in combination, the features of claims 5 and 12, the combination of *Callway* and *Conner* does not render claims 5 or 12 obvious.

Claim 14 depends from claim 1. Claim 15 depends from claim 8. Claims 14 and 15 recite similar features. Claim 14 describes mapping logic that maps a first one of the plurality of test signal groups, which was received from a first one of the plurality of multiplexers, to a first one of the plurality of outputs of the mapping logic to output as a first test output group; the mapping logic mapping a second one of the plurality of test signal groups, which was received from a second one of the plurality of multiplexers, to a second one of the plurality of outputs of the mapping logic to output as a second test

output group; and the first one of said plurality of test signal groups and the second one of the plurality of test signal groups being the same signal type of signal.

Neither *Callway* nor *Conner* describes, teaches, or suggests, either singly or in combination, the first one and the second one of the test signal groups being the same signal type of signal. *Callway* suggests that the output multiplexer 228 outputs different types of signals because *Callway* suggests that the A/D converters 208, 210, and 212 receive different types of television input signals. Because neither *Callway* nor *Conner* teaches or suggests the first one and the second one of the test signal groups being the same signal type of signal, the combination of *Callway* and *Conner* does not teach or suggest the features of claims 14 and 15; therefore, the combination of *Callway* and *Conner* does not render claims 14 or 15 obvious.

Therefore, the rejection of claims 1, 2, 5, 6, 8, 9, 12, 13, 14 and 15 under 35 U.S.C. § 103(a) has been overcome.

The Examiner has rejected claims 3 and 10 under 35 U.S.C. § 103(a) as being unpatentable over *Callway* and *Conner* and in view of *Swart*, Expandable Diaphragm Test Modules and Connectors, U.S. Patent No. 5,389,885, February 14, 1995 (hereinafter *Swart*). This rejection is respectfully traversed.

These claims describe concurrently observing test signals for a plurality of modules in combination with a plurality of multiplexers receiving specific test signals where these multiplexers combine test signals received for each test signal group to create a plurality of test signal groups, mapping logic that receives one of the test signal groups from each one of the multiplexers, and where the mapping logic maps one of the test signal groups to any one of the outputs of the mapping logic to output as a test output group.

The combination of *Callway* and *Conner* does not describe, teach, or suggest receiving specific test signals by a plurality of multiplexers in at least one module; combining, by the plurality of multiplexers, test signals received for each test signal group to create a plurality of test signal groups; receiving, by mapping logic, one of said plurality of test signal groups from each one of said plurality of multiplexers; and mapping, by said mapping logic, one of said plurality of test signal groups to any one of a plurality of outputs of said mapping logic to output as a test output group.

The Examiner relies on *Swart* to cure the deficiencies of the combination of *Callway* and *Conner*. *Swart* does not cure the deficiencies of the combination of *Callway* and *Conner*. Therefore, the combination of *Callway*, *Conner*, and *Swart* does not render Applicants' claims 3 and 10 obvious.

Therefore, the rejection of claims 3 and 10 under 35 U.S.C. § 103(a) has been overcome.

The Examiner has rejected claims 4 and 11 under 35 U.S.C. § 103(a) as being unpatentable over *Callway*, *Conner*, and *Swart* and in view of *Moore et al.*, Test Access Architecture for Testing of Circuits

Modules at an Intermediate Node Within an Integrated Circuit Chip, U.S. Patent No. 5,604,432, February 18, 1997 (hereinafter *Moore*). This rejection is respectfully traversed.

Claim 4 depends from claim 3. Claim 11 depends from claim 10.

Claims 4 and 11 describe concurrently observing test signals for a plurality of modules where the plurality of modules includes identical modules in combination with a plurality of multiplexers receiving specific test signals where these multiplexers combine test signals received for each test signal group to create a plurality of test signal groups, mapping logic that receives one of the test signal groups from each one of the multiplexers, and where the mapping logic maps one of the test signal groups to any one of the outputs of the mapping logic to output as a test output group. The combination of *Callway* and *Conner* does not describe, teach, or suggest receiving specific test signals by a plurality of multiplexers in at least one module; combining, by the plurality of multiplexers, test signals received for each test signal group to create a plurality of test signal groups; receiving, by mapping logic, one of said plurality of test signal groups from each one of said plurality of multiplexers; and mapping, by said mapping logic, one of said plurality of test signal groups to any one of a plurality of outputs of said mapping logic to output as a test output group.

The Examiner relies on the combination of *Swart* and *Moore* to cure the deficiencies of the combination of *Callway* and *Conner*. The combination of *Swart* and *Moore* does not cure the deficiencies of the combination of *Callway* and *Conner*. Therefore, the combination of *Callway*, *Conner*, *Swart* and *Moore* does not render Applicants' claims 4 and 11 obvious.

Therefore, the rejection of claims 4 and 11 under 35 U.S.C. § 103(a) has been overcome.

The remaining claims depend from the claims discussed above and are patentable for the reasons given above.

II. Conclusion

It is respectfully urged that the subject application is patentable over the cited prior art and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

Lisa Yociss

Lisa L.B. Yociss
Reg. No. 36,975
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 385-8777
Attorney for Applicants